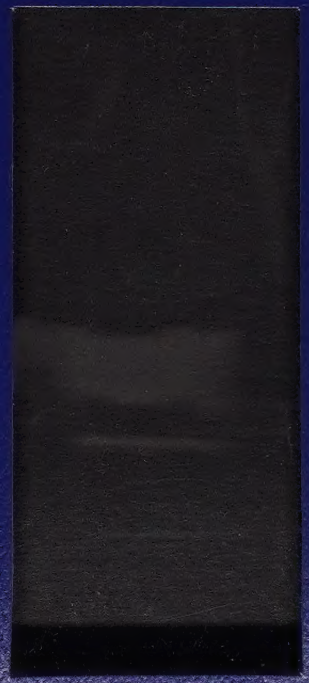
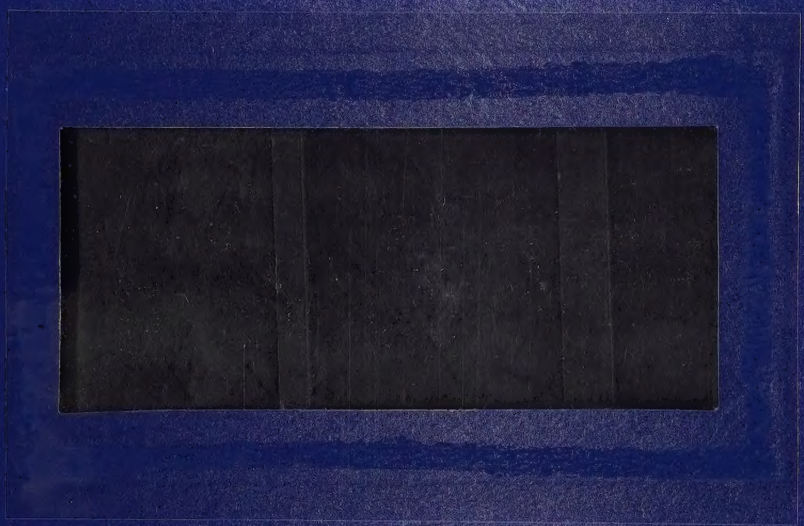




WARNING

Because of possible shock or fire hazards, connection of this instrument should be performed in compliance with the National Electric Code (ANSI C1) or any other requirements, or both, which may be applicable to the user.

Installation, operation, and maintenance should only be performed by qualified personnel.

626-PA-6030

TM-112975

VOLUME 2 -- SERVICE MANUAL

626-PA-6030

3 PHASE GRAPHIC AC MONITOR

15 September 1987

See opposite side relative to proprietary rights.

Note: Refer to Volume 1 (Operator's Manual) of TM-112975 for the installation and operation instructions.

Proprietary Information; © Copyright 1987
Dranetz Technologies, Inc.
All Rights Reserved

DRANETZ TECHNOLOGIES, INCORPORATED
1000 New Durham Rd., PO Box 4019, Edison, NJ 08818-4019

NOTICE REGARDING DRANETZ' PROPRIETARY RIGHTS

This publication contains trade secrets and other information proprietary to Dranetz Technologies, Inc. By accepting and using this manual, the user agrees that:

1. The information contained herein will be used solely for the purpose of repairing or operating equipment of Dranetz Technologies, Inc.

2. This manual will be treated as containing proprietary information and access to the manual will be limited to only those in the company organization who are responsible for the maintenance of Dranetz equipment.

3. The manuals will be returned to Dranetz Technologies, Inc. when no longer required by the user, or when there is a change in ownership of the equipment.

These publications are protected by the Copyright laws of the United States Title 17 et seq. No part of this publication may be reproduced, transcribed, stored in a retrieval system, or translated into any language or computer language, in any form, by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise, without the expressed written permission of Dranetz Technologies, Inc., 1000 New Durham Road, P.O. Box 4019 , Edison, New Jersey 08818-4019.

TABLE OF CONTENTS
626-PA-6030 3-PHASE GRAPHIC AC MONITOR

Section			Page
IV	THEORY OF OPERATION.		4-1
	4.1	Scope	4-1
	4.2	General Functional Description.	4-1
	4.3	Block Diagram Descriptions.	4-2
	4.3.1	Analog Board A1	4-2
	4.3.2	Digital Board A2.	4-2
	4.3.3	Graphics Adapter Board A3	4-5
	4.4	Analog Board A1, Detailed Description	4-5
	4.4.1	AC Input and Averaging Circuits	4-5
	4.4.2	Impulse Input and Peak Detector Circuits.	4-7
	4.4.3	Impulse Duration Comparators.	4-7
	4.5	Digital Board A2, Detailed Description.	4-7
	4.5.1	6805 Microprocessor U17 Busses and Address Decoding.	4-7
	4.5.2	Input Period Measurement.	4-9
	4.5.3	Analog to Digital Conversion.	4-9
	4.5.4	Impulse Duration Counters	4-10
	4.5.5	6502/6805 Interface Circuitry	4-10
	4.6	Graphics Adapter Board A3, Detailed Description	4-10
V	MAINTENANCE AND CALIBRATION.		5-1
	5.1	Test Equipment Recommended for Calibration.	5-1
	5.2	Preliminary Setup	5-1
	5.3	Analog Board - Common Mode Rejection	5-1
	5.4	Analog and Digital Boards - AC Level Calibration	5-2
	5.5	Analog and Digital Boards - Impulse Peak Calibration	5-3
	5.6	Graphics Adapter Board Calibration.	5-3
	5.7	System Check Adjustment	5-4
VI	REPLACEABLE PARTS LIST		
	6.1	General	6-1
	6.2	Manufacturers Codes	6-1
VII	SCHEMATIC DIAGRAMS AND ASSEMBLY DRAWINGS		7-1

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

LIST OF ILLUSTRATIONS

Figure		Page
4-1	6030 Analog Board A1, Block Diagram	4-3
4-2	6030 Digital Board A2, Block Diagram.	4-4
4-3	6030 Graphics Adapter Board A3, Block Diagram . .	4-6
7-1	626-PA-6030 3-Phase Graphic AC Monitor, Main Assembly Drawing 112975-G( ).	7-3
7-2	6030 Analog Board, Assembly Drawing 110660-G2	7-5
7-3	6030 Digital Board, Assembly Drawing 110666-G2	7-7
7-4	6030 Graphics Adapter Board, Assembly Drawing 112985-G1	7-9
7-5	6030 Analog Board A1, Schematic Diagram (Assy 110660-G2; Schematic 110665-G2)	7-11
7-6	6030 Digital Board A2, Schematic Diagram (Assy 110666-G2; Schematic 110671-G2)	7-13
7-7	Graphics Adapter Board, Schematic Diagram (Assy 112985-G1; Schematic 112990-G1.	7-15

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

IMPORTANT! CALIBRATION INTERVAL

The recommended calibration interval for this unit is once every **12 MONTHS.**

We recommend that you return the unit to the factory for calibration. If you decide to do so, first contact Dranetz Service Corp. to obtain an authorization number.

Telephone Number: (201) 755-7081
Telex Number: 499-7808
TWX Number: (710) 997-9553
FAX Number: (201) 755-0292
Cable: DRANETZ

Then fill out the Repair/Service Order form enclosed in this manual and ship it along with the unit to Dranetz Service Corp. (If this form is missing, ask Dranetz Service Corp. for a replacement.)

STATEMENT OF WARRANTY

ALL PRODUCTS OF DRANETZ TECHNOLOGIES, INC. ARE WARRANTED TO THE ORIGINAL PURCHASER AGAINST DEFECTIVE MATERIAL AND WORKMANSHIP FOR A PERIOD OF ONE YEAR FROM THE DATE OF DELIVERY. DRANETZ WILL REPAIR OR REPLACE, AT ITS OPTION, ALL DEFECTIVE EQUIPMENT RETURNED, FREIGHT PREPAID, DURING THE WARRANTY PERIOD, WITHOUT CHARGE FOR REPAIR, PROVIDED THERE IS NO EVIDENCE THAT THE EQUIPMENT HAS BEEN MISHANDLED OR ABUSED. THIS WARRANTY SHALL NOT APPLY TO ANY DEFECTS RESULTING FROM IMPROPER OR INADEQUATE MAINTENANCE, BUYER-SUPPLIED HARDWARE/SOFTWARE OR INTERFACING, UNAUTHORIZED MODIFICATION OR MISUSE OF THE EQUIPMENT, OPERATION OUTSIDE OF THE ENVIRONMENTAL SPECIFICATIONS FOR THE PRODUCT, OR IMPROPER SITE PREPARATION OR MAINTENANCE.

The information in this manual has been reviewed and is believed to be entirely reliable. No responsibility, however, is assumed for any inaccuracies. The material in this manual is for information purposes only, and is subject to change without notice.

VOLUME 2
SERVICE MANUAL

626-PA-6030 3-PHASE GRAPHIC AC MONITOR

SECTION IV
THEORY OF OPERATION

4.1 SCOPE

Volume 2 of TM-112975 provides the service, calibration, and maintenance instructions for the 626-PA-6030 3-Phase Graphic AC Monitor, hereinafter referred to as the 6030 plug-in. This volume is divided into four sections: (IV) THEORY OF OPERATION, (V) MAINTENANCE AND CALIBRATION, (VI) REPLACEABLE PARTS LIST, and (VII) SCHEMATICS AND ASSEMBLY DRAWINGS. See Volume 1 of TM-112975 for the installation and operation instructions.

4.2 GENERAL FUNCTIONAL DESCRIPTION

The 6030 plug-in is designed to monitor up to three phases of AC power lines and provide disturbance data in both text and graphical form. Physically, the 6030 consists of three circuit boards which occupy two plug-in slots of the Series 626 mainframe. The Analog board contains three channels of analog circuitry (one per AC phase) used for the text information. The Graphics Adapter board consists of three channels of sampling circuits for obtaining the graphics data. The Digital board oversees the control and data tasks.

The AC signal is fed into the Analog and Graphics Adapter boards simultaneously. Circuits in the Analog board obtain information on the time average and peak values of the AC waveform. This data is made available to the Digital board where the values are compared to the user set thresholds. If a threshold is exceeded, the information is put on the main CPU stack. Simultaneously, the Graphics Adapter board is signalled that an event has occurred. The Graphics Adapter board samples the incoming AC waveform continuously and stores those samples in its own memory. When it is signalled by the Digital board that an event has occurred, the Graphics Adapter board sets aside the samples containing the cycle in which the event was detected as well as the samples for one cycle on either side of that event cycle.

When the event is printed out, the text information is first printed, followed by the graphic data. Limited memory is available for the storage of graphic data. When all of the available memory is used, no additional graphics data is stored until sufficient memory is free. During such intervals, events will still be printed out, but in text form only.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

4.3 BLOCK DIAGRAM DESCRIPTIONS

4.3.1 Analog Board A1

Figure 4-1 is a block diagram of the phase A circuits in the Analog board. (The phase B and phase C circuits are configured in identical fashion.) The phase A input signal is applied to both the AC level and impulse sections of the phase A circuits. In the AC level section, AC signals are isolated and attenuated, then low pass filtered. In the phase A channel only, the filtered output passes to the Digital board where it is used as a frequency reference for frequency measurement. In the Analog board, the filtered signal is full wave rectified and integrated. In the track/hold circuit, the integrated output is sampled by the FOLLOW signal at the start of a measurement cycle. When the RESET signal appears, the sampled voltage is transferred to the Digital board.

In the impulse section, inputs are attenuated, buffered and notch filtered to remove the AC fundamental. The notch frequency range is controlled by a RANGE signal from the Digital board. The filtered signal is applied to a rectifying peak detector whose output, representing the phase A pulse level, is buffered and routed to the Digital board. The peak detector is reset after the pulse value is read. The duration comparators notify the Digital board when the measured pulses exceed preset limits (in either the positive or negative direction, depending on the polarity of the pulse being monitored).

4.3.2 Digital Board A2 (See fig. 4-2.)

The Digital board houses the 6805 CPU, two 4K-byte PROMs (one for each CPU), the 6502/6805 interface, an analog-to-digital converter, an analog multiplexer, a self-test signal generator, and counters for frequency and impulse duration measurement. The 6805 processor in the Digital board takes measurements and detects disturbances. The 626 Mainframe CPU, a 6502, does the actual printing of events and programming of limits. The two processors communicate with each other through a parallel interface.

The 6805 processor operates in conjunction with an 8-bit data bus and a 13-bit address bus. A 4K byte PROM occupies half of the 6805's addressing range. The phase A frequency signal supplied by the Analog board is applied to an impulse period counter. Period counts from four consecutive cycles are summed and fed to timers of the Versatile Interface Adapter.

An A/D converter in the Digital board receives multiplexed AC levels and impulse amplitudes from the phase A, B, and C circuits in the Analog board. Two references are made available to the A/D converter to accommodate whichever input is received by the converter.

The 6805 processor provides a RANGE signal to the Analog board. The logic level of this signal controls the two ranges of the reference and AC integrators.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

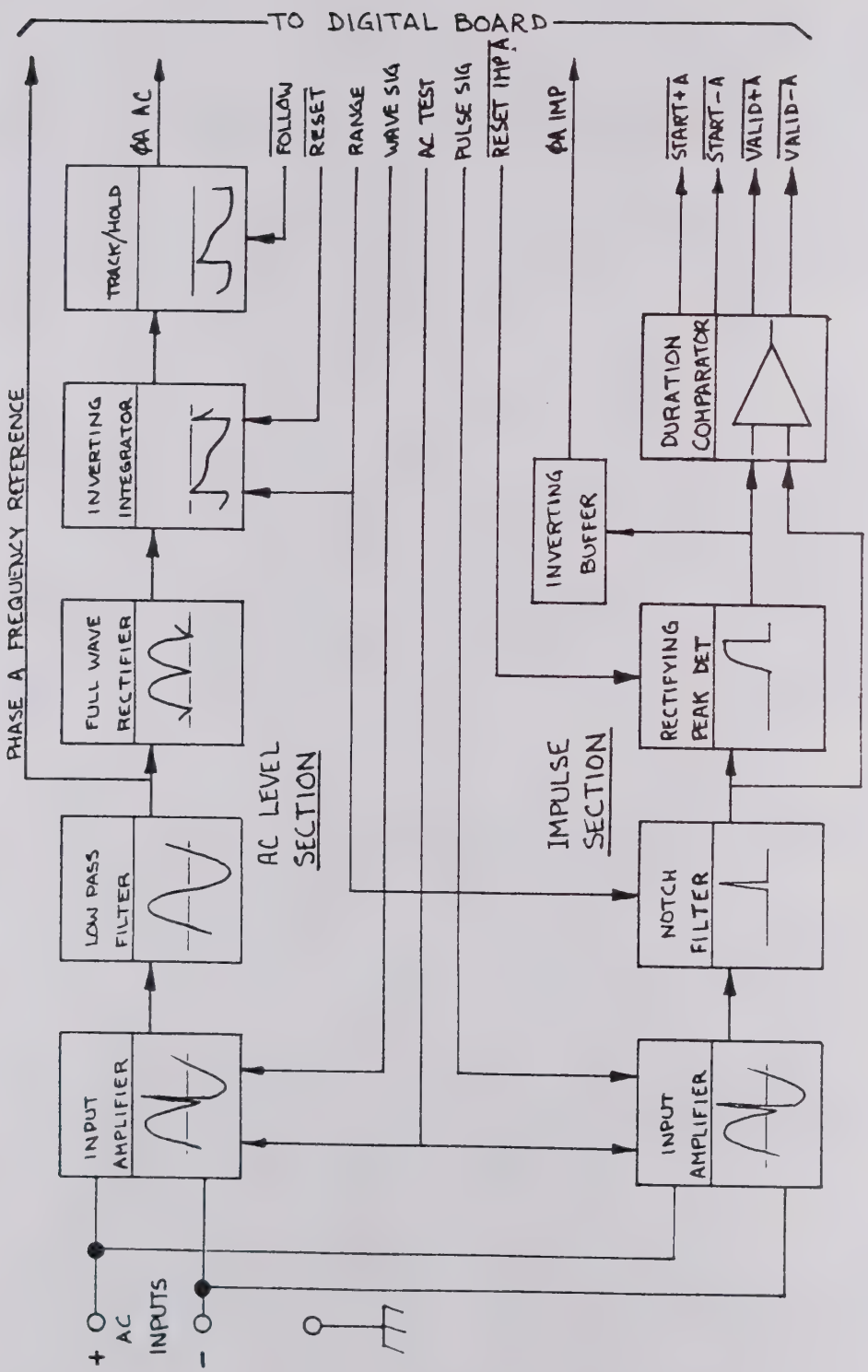


Figure 4-1. 6030 Analog Board A1, Block Diagram

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

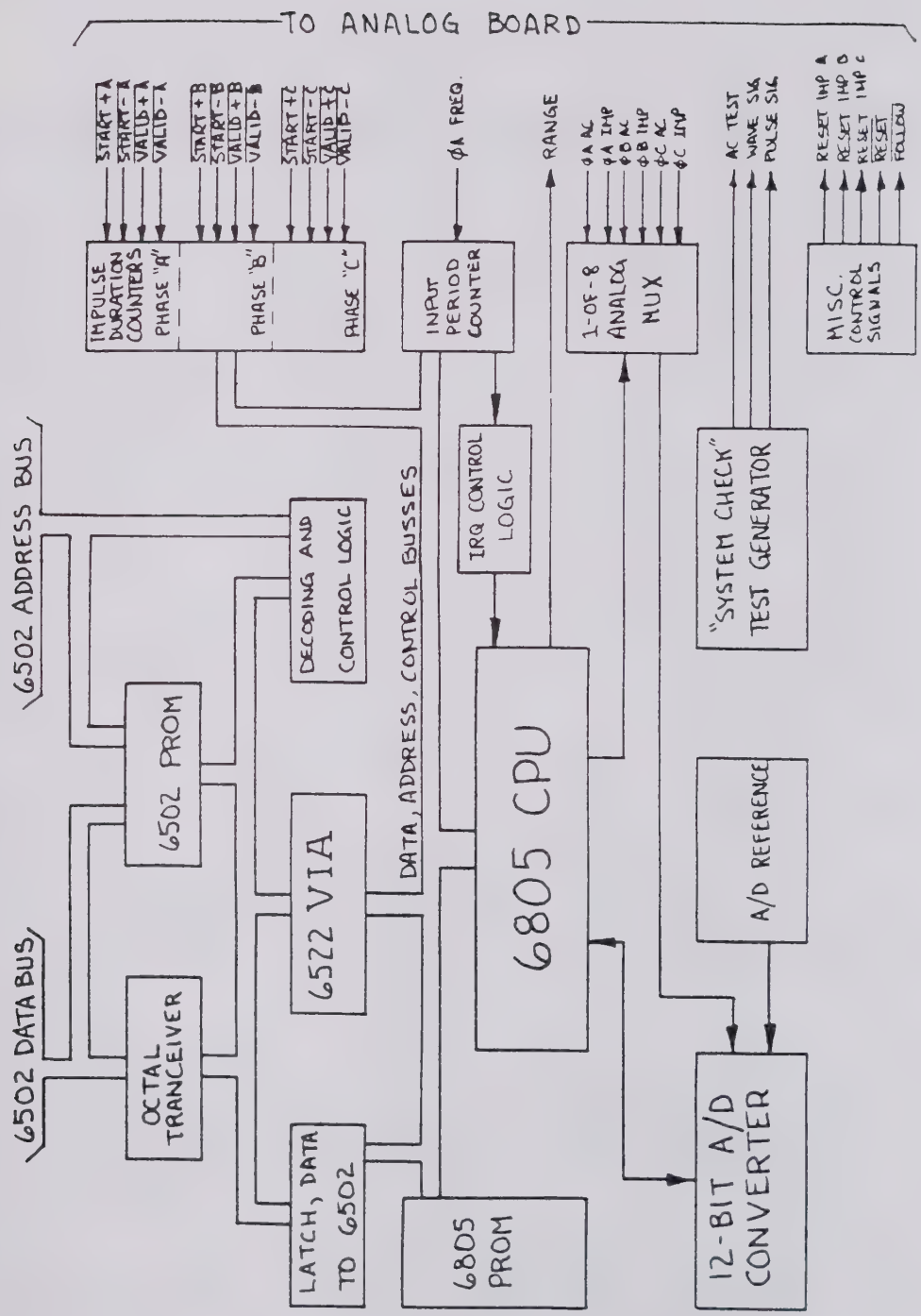


Figure 4-2. 6030 Digital Board A2, Block Diagram

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

Four control signals from each of the three duration comparators on the Analog board are applied to the impulse duration counters on the Digital board. Counts representing the duration of the monitored pulses above or below given threshold values, as well as a signal representing pulse polarity, are latched and made available to the 6805 processor.

The Digital board also contains the 6502/6805 interface circuits which consist of two latches, a handshake line and associated control logic. The circuits are configured to enable either processor to transmit bytes to the other. The handshake line ensures that information passes in either direction without interruption.

4.3.3 Graphics Adapter Board A3 (See fig. 4-3.)

The AC input signal first passes through a wideband attenuator to reduce the signal to more practical levels for measurement. The attenuated signal is then applied through input and variable gain amplifiers to two peak detectors, one responding to positive-going signals and the other to negative-going signals. Every 128 microseconds, the peak detector outputs are read and then reset. Using peak detectors in the sampling circuits enables the detection of transients that otherwise would be missed at this sampling rate. The signals from the peak detectors are fed to analog-to-digital converters which are read by the 6303 CPU. These values are stored for possible later use. All of the timing and control signals for the peak detectors and A/D conversion, as well as the required memory and interface signals, are controlled by the onboard CPU.

Two bidirectional 8-bit ports are used for communication between the Graphics Adapter and Digital boards and the 6502 mainframe processor. One of these ports is used exclusively for communication between the Graphics and Digital boards during interrupt service.

4.4 ANALOG BOARD A1, DETAILED DESCRIPTION (SEE FIG. 7-5.)

NOTE

Since most of this board consists of three identical sections (one for each AC phase), the following description is keyed to phase A, but applies equally to phases B and C except where noted.

4.4.1 AC Input and Averaging Circuits

The input amplifier (output signal at U1A, pin 1) provides isolation and attenuation. R8A and C2A are common-mode rejection adjustments. During a "System Check" sequence, the input signals are blocked at U15A, pins 11 and 14, and a square-wave AC signal is injected at point PA. R76A controls the AC value printed during the "System Check".

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

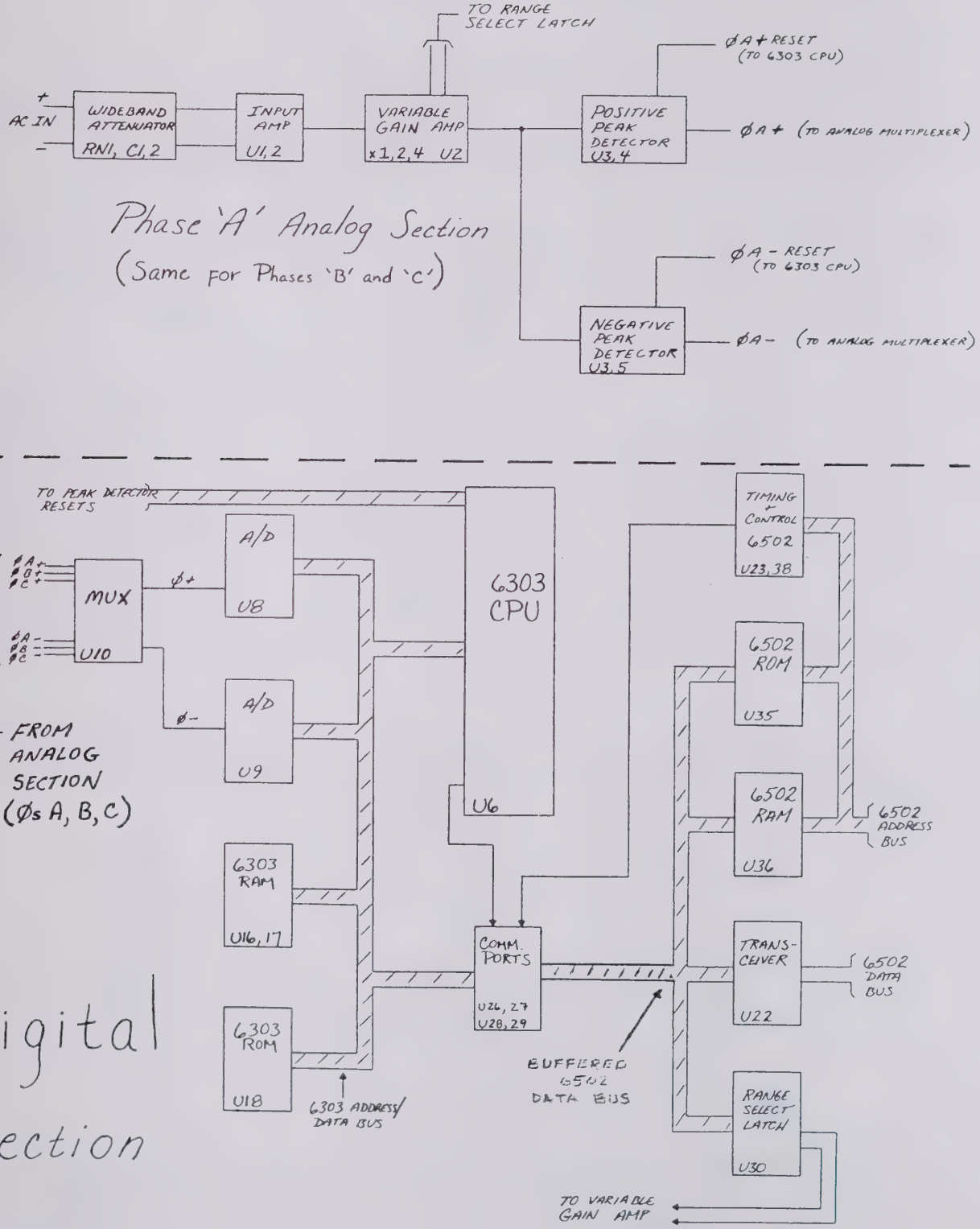


Figure 4-3. 6030 Graphics Adapter Board A3, Block Diagram

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

The signal from the input amplifier passes through a low-pass filter (U2A, pin 1). On phase A only, this output is used for frequency measurement. The signal is rectified (U3A, pin 1) and integrated (U3A, pin 7). R17A is a balance trimmer and R23A is an offset adjustment. R25A and R93A are gain trimmers. At the start of a measurement cycle, the FOLLOW signal from the Digital board goes high, opening a switch (U10A) and leaving C15A charged with a voltage equal to the output of the integrator. The RESET signal then goes low, discharging the integrator capacitor C14A through another switch (U10A). Voltage on C15A is buffered (U4A, pin 1) and sent to the analog multiplexer on the Digital board.

4.4.2 Impulse Input and Peak Detector Circuits

Inputs are attenuated by capacitive voltage dividers and buffered (U6A, pin 1). C26A and R32A are common mode rejection trimmers. During System Check, a pulse is injected at point OA. R72A controls the System Check impulse amplitude. A notch filter (U6A, pin 7) removes the AC fundamental. The center frequency is 390 Hz if RANGE is high and 430 Hz if RANGE is low. A rectifying peak detector charges capacitor C35A whose output is buffered by Q1A. R43A establishes the operating point of Q1A. The source of Q1A is buffered (U5A, pin 7), inverted (U4A, pin 7) and fed to the multiplexer. R41A is a balance adjustment, R63A is a gain control and R65A is an offset trimmer. The peak detector is reset when the impulse duration counter is read by the 6805.

4.4.3 Impulse Duration Comparators

Comparator outputs (U9A) control the duration counters on the Digital board. Pin 2 (for positive pulses) or pin 8 (for negative pulses) will go low during impulses greater than either 25 volts or 10% of the value stored in the peak detector. The counters are active when either signal is low. Pin 16 (positive) or pin 10 (negative) goes low if the new amplitude exceeds that stored in the peak detector, allowing the count to be latched.

4.5 DIGITAL BOARD A2, DETAILED DESCRIPTION (SEE FIG. 7-6)

4.5.1 6805 Microprocessor U17 Busses and Addresses Decoding

The 6805 multiplexes the low-order address byte with its 8-bit data bus. A complete 13-bit address bus is created by using U11 to latch valid addresses on the falling edge of the ADDRESS STROBE signal (U3, pin 6). All hardware connected to the data bus is gated so that there is no bus contention during the setup of addresses. The 4K-byte PROM used by the 6805 occupies half of its addressing range, and is selected when output A12 of U17 goes high. Table 4-1 is the 6805 CPU memory map.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

Table 4-1. Memory Map for 6805 CPU

Hex Address	Use
$\overline{0000}$	6805 I/O port A
Bit 7	Input, handshake line
Bit 6	Output, test pulse control
Bit 5	Output, A/D converter mode control
Bit 4	Input, A/D status
Bits 3-0	Inputs, high and low nibbles of A/D data
0001	6805 I/O port B
Bits 7-4	Inputs, middle nibble of A/D data
Bit 3	Output, frequency range control
Bits 2-0	Outputs, analog MUX address, A/D ref. control
0004	6805 port A data direction register
0005	6805 port B data direction register
0008	6805 internal timer
0009	6805 internal timer control register
0010-007F	6805 internal RAM
0080	Read, imp. dur. high byte (bit 7 is polarity), ph. A (hardware causes FOLLOW signal to go low)
0081	Read, imp. dur. low byte, ph. A (hardware resets ph. A imp. peak detector)
0082-0085	Same as 0080-0081 for ph. B & C, FOLLOW not affected.
0088	Write, data to be read by 6502 (hardware causes HANDSHAKE to go high)
0089	Read, data ignored (hardware starts A/D converter)
008A	Read, data ignored (hardware causes 6502 interrupt line to go low)
0090-009F	6522 VIA addresses
1000-1FFF	6805 software

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

4.5.2 Input Period Measurement

The filtered waveform from phase A is squared (U54, pin 1) and fed to a comparator (U48) which performs a logic level translation. The rising edge of the comparator output triggers a one-shot (U47), causing the outputs of counters U27 and U28 to be saved by latches U25 and U26. The end of the one-shot pulse triggers another one-shot (U47), resetting the counters and interrupting the 6805, which reads the count. Reading U26 removes the interrupt request. Period counts from four consecutive cycles are added together, and the sum is used to set one of the timers of the Versatile Interface Adapter (U7). The 6805 will be interrupted each time the VIA timer runs out, or once every measurement cycle. The $\overline{\text{RESET}}$ and $\overline{\text{FOLLOW}}$ signals are derived directly from the VIA interrupt request pin (U7, pin 21).

4.5.3 Analog to Digital Conversion

Six voltage measurements are made every measurement cycle, representing the AC levels and impulse amplitudes for each of the three phases. A multiplexer (U53) allows one signal at a time to be applied to the A/D converter input (U18, pin 13). The state of pins 34, 35, and 36 of U17 determine which signal is chosen. Voltage at the multiplexer output (U35, pin 8) is buffered (U33, pin 1) and inverted (U33, pin 7) so that only positive voltages are applied to the A/D input. R20 is an offset adjustment.

The A/D converter uses two reference voltages. One is constant, used for measurement of impulse peaks. The other varies with the measurement period, and is used when measuring AC level. The level at U17 pin 36 and its complement at U29 pin 10 turn on either one of two switches (U31), causing the proper voltage to appear at U30 pin 5. This signal is slightly amplified (U30, pin 7) and sent to the A/D reference input (U18, pin 10).

The constant reference is derived from the A/D REF OUT pin (U18, pin 8). R8 is adjusted to calibrate this reference. To obtain the variable reference, the voltage across zener diode CR4 is integrated, resulting in a ramp waveform at U34 pin 1. During the measurement period, the integrator output voltage is gated through switch U31, allowing the voltage across capacitor C35 to follow the integrator output. At the end of the measurement period, when $\overline{\text{FOLLOW}}$ goes high, C35 is left charged to the highest voltage reached by the integrator, and the integrator is reset. U34 pin 7 is used to buffer C35.

The reference integrator and the AC integrators on the Analog board operate over two ranges, controlled by the RANGE signal (U17, pin 33). The 6805 controls this line based on the input frequency of phase A. The RANGE signal should be at a logic high for frequencies of 409 Hz and below (low range), and low for frequencies of 411 Hz and above (high range). The center frequency of the notch filters on the Analog board is also affected by this line. R23 and R25 are used to calibrate the variable reference for the low and high frequency ranges, respectively.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

4.5.4 Impulse Duration Counters

NOTE

The following description is keyed to the circuit for phase A, but applies identically to corresponding circuits for phases B and C.

The impulse duration counters are controlled by signals from the Analog board. Each phase has four control signals called $\overline{\text{START+}}$, $\overline{\text{VALID+}}$, $\overline{\text{START-}}$, and $\overline{\text{VALID-}}$. Either $\overline{\text{START}}$ line will go low for any impulse greater than 25 volts, and will stay low until the amplitude drops below about 10% of the voltage stored in the peak detector. The $\overline{\text{VALID}}$ signals go low only if the incoming pulse is greater in amplitude than that stored in the peak detector so far.

Two dual 4-bit counters, U23 and U20, are configured as one 12-bit counter which will stop on an overflow condition. As long as both START signals are high, the counter is in a reset condition (all zeros). As long as either $\overline{\text{START}}$ signal is low, the counter increments at a 1 MHz rate derived from the 6502 "phase 2" clock. The output of the counter is connected to the inputs of tri-state latches U24 and U21. A count is latched on a positive-going edge of U22 pin 8, which is normally high. This line goes low only when a $\overline{\text{START}}$ and a $\overline{\text{VALID}}$ signal are active at the same time, and will go high again when either signal returns to an inactive state, causing the counter to be latched. The $\overline{\text{VALID}}$ signals also determine the polarity of the impulse, which is latched with the count.

4.5.5 6502/6805 Interface Circuitry

Two latches, a handshake line, and assorted control logic make up the interface circuit. When the 6502 sends a byte to the 6805, the byte is latched into port A of the VIA (U7) and the handshake line (U9, pin 4) goes low. When the 6805 reads the byte from port A, the handshake line goes high. The 6805 writes data into latch U8, bringing the handshake high, and when the 6502 reads the data from U8, the handshake goes low. When a number of bytes are to be transferred, the processor doing the sending will always wait for the handshake line to change before sending the next byte.

4.6 GRAPHICS ADAPTER BOARD A3, DETAILED DESCRIPTION (SEE FIG. 7-7.)

NOTE

The following description is keyed to the circuit for phase A, but applies identically to corresponding circuits for phases B and C.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

The AC input signal is applied to wideband attenuators RN1A/C1A/C2A and RN2A/C3A/C4A reducing signal levels to those more appropriate for use in the following circuits. Diodes CR1-CR4 clamp the attenuated inputs to ±7.5 VDC to prevent overdriving the inputs of operational amplifiers U1A and the degradation of its common mode rejection ratio. Operational amplifiers U1A and U2A-7 form a differential amplifier where potentiometers R8 and R11 are used to set the common mode rejection ratio and gain, respectively. The output of amplifier U2A-7 feeds operational amplifier U2A-1 which, in conjunction with analog switch U3A, provides a selectable gain of 1, 2, or 4 from which the input ranges of 1000, 500, or 250 volts peak are derived. The signal is then fed into two peak detectors (U4 and U5), one responding to positive peaks and the other to negative peaks. The peak detectors are reset at approximately an 8 kHz rate by analog switch U3. Potentiometers R20A and R25A are used to set up a 2.5 VDC offset which is summed with the peak detector outputs to feed the single supply A/D converters U8 and U9. The 5.0 VDC reference for the A/D converter is derived from U21-7.

The output of one-shot U11, at pin 4, is gated with OR gate U19-3 to provide the reset pulse of the peak detectors. This reset pulse occurs coincident with the reading of the A/D converters. The time between samples, approximately 128 uSeconds, is controlled by CPU U6. The memory has a 12-cycle capacity which is continuously being rewritten. A new cycle is initiated at every sync pulse (U6-20). This pulse is derived from a similar pulse originating on the Analog board.

Two bidirectional ports (U26/U27 and U28/U29) are provided for communication. Port U26/U27 is used for communication between the Graphics Adapter and Digital boards during the interrupt service routine. The second port is used for general communications and data transfer between the Graphics Adapter board, the mainframe processor and the Digital board.

At the end of each cycle, the 6303 processor (U6) writes a code into U27 that is read by the 6502 mainframe processor. If an event has occurred, this code will be echoed back via U26. This signals the Graphic Adapter board to save that particular cycle of data, as well as the cycle before and after. Just before the event is printed, these samples are transferred to a different RAM (U36). This frees up to three cycles of memory which can then be used to store additional events.

If events occur rapidly enough, the 12 cycles of memory will all be full of data. When this occurs, the sampling system shuts down and waits until three cycles of memory are free. Once three cycles are free, sampling will be resumed.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

SECTION V
MAINTENANCE AND CALIBRATION

5.1 TEST EQUIPMENT RECOMMENDED FOR CALIBRATION

The following items of test equipment are recommended for calibration:

1) Wide bandwidth oscilloscope
2) 10 megohm attenuator probes (2) for oscilloscope
3) High voltage probe for oscilloscope
4) AC voltage source, 0-600V rms, 350-450 Hz
5) AC voltmeter to measure up to 600V rms
6) High voltage pulse generator, variable duration
7) Peak reading voltmeter
8) CRT data terminal set for 9600 baud

5.2 PRELIMINARY SETUP

With 626 power turned off, remove the communications panel and the CPU board, set the baud rate DIP switch to position "E" (9600 baud), then replace the CPU board and panel. Install a long extender card in one of the plug-in slots of a 626 mainframe. Remove the four screws on the Digital board that hold the Digital board to the Analog board and connect the plug-in to the extender so that the Analog and Graphics Adapter boards lie on the bench. Mount a standoff on the Digital board at the lower standoff hole near the edge plugged into the extender. Attach heavy braided conductor between this standoff and the corresponding one on the Analog board. Braid should also be connected between the plug-in's rear panel sheet metal and the metal frame of the 626. Adjust R43A, B, and C on the Analog board fully counterclockwise and center all other variable resistors. Connect the three "+" inputs together and the "-" inputs together so that all three phases receive the same signals during calibration. Connect the CRT terminal to the 626 RS-232C port, power up the 626, and disable the printer.

NOTE

Since many component designations in the Analog and Gaphics Adapter boards use a phase letter A, B, or C, the letter "X" will be used to represent such letters. For example, instead of "U1A, B, and C", the term "U1X" will be used.

5.3 ANALOG BOARD - COMMON MODE REJECTION

Connect the AC source to the Analog board so that 300V at 400 Hz is applied to both the "+" and "-" inputs of all three phases with respect to the 626 case ground. Adjust C2X and R8X so that the signals at U1X pin 1 are at a minimum (no more than 15 mV p-p). In most cases, it should be possible to achieve a null of less than 5 mV.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

Adjust R32X for minimum signal at U6X pin 1. Remove the AC source and connect the pulse generator so that clean half-sine pulses of 1000 volts peak at 10 uSec duration are applied to both the "+" and "-" inputs of all three phases with respect to the 626 case ground. Adjust C26X for a minimum signal at U6X of no more than 15 mV peak.

5.4 ANALOG AND DIGITAL BOARDS - AC LEVEL CALIBRATION

NOTE

Most adjustments will be made on the Analog board except when the Digital board is specified.

1) Connect the AC source to apply 300V at 400 Hz differentially across the "+" and "-" inputs.

2) Place the 626 in the PROGRAM mode, select the proper channel, and turn the PRINTOUT MODE switch to the SYSTEM CHECK position. A constant readout of voltage and frequency should appear on the CRT.

3) Increase the frequency to 430 Hz and verify that the CRT readout follows the frequency change and that the RANGE signal is low.

4) Adjust R25 on the Digital board so that all voltage reading are approximately 300 volts.

5) Adjust R25X so that all three channels read accurately to within 0.6 volts.

6) Lower the input frequency to 390 Hz and verify that RANGE goes high.

7) Adjust R23 on the Digital board so that all voltage readings are approximately 300 volts.

8) Adjust R93X to bring individual phases in agreement.

9) Set the input to 50 volts and adjust R23X to calibrate individual channels.

10) Repeat the above sequence one or two more times, starting with 300V at 430 Hz and setting R25X, lowering the frequency to 390 Hz and setting R93X, then lowering the voltage to 50V and setting R23X.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

5.5 ANALOG AND DIGITAL BOARDS - IMPULSE PEAK CALIBRATION

1) Remove all input sources and set the oscilloscope to trigger on the rising edge of the signal at U18 pin 28 on the Digital board, using a sweep of about 2 mSec per division.

2) The signal at U5X pin 7 should be at a minimum very soon after the trigger and rise to a level of a few millivolts until just before the next trigger. Adjust R43X clockwise until a rise of about 25 mV is observed.

3) Connect the pulse generator to apply 1000V, 10 uSec differential pulses so that polarity is positive with respect to the "+" and "-" inputs.

4) Program the plug-in for a 50-volt impulse threshold and place the 626 in the OPERATE mode.

5) While applying pulses, set R8 on the Digital board so that all phases read approximately 1000 volts, then adjust R63X for calibration of individual phases.

6) Reverse the polarity of the applied pulses and adjust R41X so that all phases read correctly.

7) Reduce the amplitude to 100 volts and switch the polarity back to positive.

8) Adjust R65X so that all phases read correctly.

9) Check again for acceptable reading for 1000 volts at both polarities and readjust as necessary.

5.6 GRAPHICS ADAPTER BOARD CALIBRATION

1) Install 6030 plug-in on two plug-in extender cards, P/N 110260.

2) Select 250 Vpk graph range.

3) Apply a 150 Vrms, 60 Hz sinusoidal waveform between the "-" input and ground. (Use a signal generator/power amplifier combination whose distortion does not exceed 1%.)

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

4) Adjust R11X for a reading of 1.5 Vrms ±0.5% at U4-1.

5) Turn off signal source.

6) Apply a 150 Vrms 60 Hz signal from the "+" input to ground.

7) Adjust R8X for a reading of 1.5 Vrms ±0.5% at U4-1.

8) Check the voltage at U5-1. It should read 1.5 Vrms ±2.5%.

9) Turn off signal source.

10) Adjust R20 for a reading of 2.5 Vdc ±0.5Vdc at U4-1.

11) Adjust R25X for a reading of 2.5 Vdc ±0.5% at U5-1.

12) Adjust R32 for a reading of 5.00 Vdc.

5.7 SYSTEM CHECK ADJUSTMENT

1) Remove all plug-in inputs and set the 626 to produce continuous SYSTEM CHECK printouts.

2) Adjust R42 on the Digital board so that the AC readings are all approximately 200 volts.

3) Set R76X on the Analog board so that all AC values are as close as possible to 200.0 volts.

4) Adjust R72X on the Analog board so that all impulse peaks read close to 2000 volts.

5) AC readings must stay within 1% of 200V and impulse values must stay within 10% of 2000V. Impulse polarity should always be negative and duration should be between 9 and 11 uSec. The frequency should read between 399.5 and 400.5 Hz.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

SECTION VI
REPLACEABLE PARTS LIST

6.1 GENERAL

The replaceable parts list identifies the replaceable parts in the 6030 plug-in. For each replaceable part, the following is presented: reference designation (if applicable), part number, manufacturer's code number, and description. Hardware is not included in this table. For information concerning the hardware, contact the Dranetz Service Corporation.

Refer to figures 7-1 through 7-3 for the location of the replaceable parts referenced in the parts list.

6.2 MANUFACTURERS CODES

The manufacturers codes referenced in the Replaceable Parts List that follows are identified below.

Man. Code	Source
00779	Amp, Inc., P.O. Box 3608 Harrisburg, PA 17105
23207	Dranetz Technologies, Inc. 1000 New Durham Road, P.O. Box 4019 Edison, New Jersey 08818-4019 (201) 287-3680
81349	On Mil specification list. Manufactured to meet military specifications. Available from a variety of suppliers.

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Main Assembly, P/N 112975-G( )

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
A1	110660-G2	23207	Analog PC Board Assy
A2	110666-G2	23207	Digital PC Board Assy
A3	112985-G1	23207	Graphic Adapter PC Board Assy
J1-J3*	1-480701-0	00779	Connector Housing (3)
	350690-1	00779	Pin Contacts (9)
L1A,B,C L2A,B,C	104619	23207	Ferrite Bead
R1A,B,C R2A,B,C	RCR07G102J	81349	Res, 1K, 5%, 1/4W
	103253-G7**	23207	Terminal Block
	110278**	23207 Cover	Rear Input Terminal
	5646-190-44	00779	Jumper Cable (2)
	110480-G1* or -G2* (As ordered)	23207	626 AC Module Cable Assy

---

*Used in -G2 version only
**Used in -G1 version only

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Analog Board A1, P/N 110660-G2

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
C1A,B,C	104026-G8	23207	Cap, 22 pf, 5%, 500V
C2A,B,C C26A,B,C	104109-G3	23207	Cap, Var, 6.5-30 pf, 100V
C3A,B,C C6A,B,C C16A,B,C C17A,B,C C27A,B,C C32A,B,C C34A,B,C C36A,B,C C37A,B,C C38A,B,C C39A,B,C C44A,B,C C54,C55,C56, C59A,B,C C60A,B,C C61A,B,C C62A,B,C C63A,B,C C64A,B,C	103209-G3	23207	Cap, 0.47 uf, 20%, 50V
C4A,B,C	104019-G4	23207	Cap, 330 pf, 1%, 500V
C5A,B,C	104110-G4	23207	Cap, .0033 uf, 2%, 50V
C7A,B,C	104021-G6	23207	Cap, 1000 pf, 2%, 100V
C8A,B,C	104110-G3	23207	Cap, .0015 uf, 2%, 50V
C10A,B,C C57	104067-G5	23207	Cap, 10 uf, 5%, 6V
C14A,B,C	104110-G1	23207	Cap, .022 uf, 2%, 50

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Analog Board A1, P/N 110660-G2 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
C15A,B,C C29A,B,C C30A,B,C C31A,B,C	104110-G6	23207	Cap, .015 uf, 2%, 50V
C18A,A19A C18B,C19B C18C,C19C	104115	23207	Matched Pair, Cap, 50 pf, 3 KV
C20A,C21A C20C,C21C	104122 C20B,C21B	23207	Matched Pair, Cap, .033 uf, 2%, 50V
C65	104110-G1	23207	Cap, .022 uf, 2%, 50V
C22A,B,C C23A,B,C C24A,B,C C49A,B,C	104111-G3	23207	Cap, 75 pf, 2%, 500V
C25A,B,C	104027-G1	23207	Cap, 50 pf, 5%, 500V
C35A,B,C	104030-G7	23207	Cap, .0056 uf, 10%, 80V
C40A,B,C C41A,B,C	104017-G5	23207	Cap, 36 pf, 5%, 500V
C52,C53	104067-G7	23207	Cap, 33 pf, 10%, 16V
C65	104110-G1	23207	Cap, .022 uf, 2%, 50V
CR1A,B,C CR2A,B,C CR3A,B,C CR5A,B,C CR7A,B,C CR8A,B,C	104412-G2	23207	Diode, High Speed Switching
L1A,B,C L2A,B,C	104620	23207	Ferrite Bead
Q1A,B,C	104539	23207	Field Effect Transistor

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Analog Board A1, P/N 110660-G2 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
Q2A,B,C Q3A,B,C	104505	23207	Transistor, NPN, SIL, Audio
R1A,B,C R2A,B,C	104711	23207	Resistor Network
R3A,B,C R4A,B,C	RN55C3013F	81349	Res, 301K, 1%, 1/10W
R5A,B,C R6A,B,C R21A,B,C R38A,B,C R39A,B,C R46A,B,C R71	RN55C1002F	81349	Res, 10K, 1%, 1/10W
R7A,B,C	RN55C2492F	81349	Res, 24.9K, 1%, 1/10W
R8A,B,C R25A,B,C R63A,B,C R76A,B,C	104719-G5	23207	Res, Var, 50K, 10%, 1/2W
R9A,B,C	RN55D1214F	81349	Res, 1.21 Meg, 1%, 1/10W
R11A,B,C	RN55C3323F	81349	Res, 332K, 1%, 1/10W
R12A,B,C	RN55C9093F	81349	Res, 909K, 1%, 1/10W

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Analog Board A1, P/N 110660-G2 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
R13A,B,C	RN55C3243F	81349	Res, 324K, 1%, 1/10W
R16A,B,C	RN55C1962F	81349	Res, 19.6K, 1%, 1/10W
R17A,B,C	104719-G6	23207	Res, Var, 1K, 10%, 1/2W
R22A,B,C R64A,B,C	RN55D1005F	81349	Res, 10 Meg, 1%, 1/10W
R23A,B,C R65A,B,C R72A,B,C R93A,B,C	104719-G7	23207	Res, Var, 100K, 10%, 1/2W
R24A,B,C	RN55C2002F	81349	Res, 20K, 1%, 1/10W
R26A,B,C	RN55C4023F	81349	Res, 402K, 1%, 1/10W
R27A,B,C	RN55C1000F	81349	Res, 100 ohms, 1%, 1/10W
R28A,B,C R29A,B,C R30A,B,C R70A,B,C	RN55D1004F	81349	Res, 1 Meg, 1%, 1/10W
R31A,B,C	RN55C7503F	81349	Res, 750K, 1%, 1/10W
R32A,B,C	104719-G9	23207	Res, Var, 500K, 10%, 1/2W

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Analog Board A1, P/N 110660-G2 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
R34A,B,C R35A,B,C	RN55C3013F	81349	Res, 301K, 1%, 1/10W
R37A,B,C	RN55C7502F	81349	Res, 75K, 1%, 1/10W
R40A,B,C	RN55C49R9F	81349	Res, 49.9 ohms, 1%, 1/10W
R41A,B,C R43,B,C	104719-G2	23207	Res, Var, 5K, 10%, 1/2W
R42A,B,C	RN55C7501F	81349	Res, 7.5K, 1%, 1/10W
R44A,B,C	RN55C2001F	81349	Res, 2K, 1%, 1/10W
R49A,B,C	RN55C3012F	81349	Res, 30.1K, 1%, 1/10W
R51A,B,C	RN55D1434F	81349	Res, 1.43 Meg, 1%, 1/10W
R52A,B,C	RN55C2742F	81349	Res, 27.4K, 1%, 1/10W
R54A,B,C	RN55D1584F	81349	Res, 1.58 Meg, 1%, 1/10W
R55A,B,C	RN55C3322F	81349	Res, 33.2K, 1%, 1/10W
R61A,B,C	RN55C3651F	81349	Res, 3.65K, 1%, 1/10W
R62A,B,C	RN55C4992F	81349	Res, 49.9K, 1%, 1/10W
R66A,B,C	RN55C1003F	81349	Res, 100K, 1%, 1/10W

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Analog Board A1, P/N 110660-G2 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
R75A,B,C	RN55C6813F	81349	Res, 681K, 1%, 1/10W
R90A,B,C R91A,B,C	RN55D1474F	81349	Res, 1.47 Meg, 1%, 1/10W
R92A,B,C	RN55C4642F	81349	Res, 46.4K, 1%, 1/10W
R94A,B,C	RN55C2000F	81349	Res, 200 ohms, 1%, 1/10W
RN1A,B,C	104723	23207	Res Netwk, 22K, 2%
RN2A,B,C RN3A,B,C	104724	23207	Res Netwk, 3.3K, 2%
U1A,B,C U2A,B,C U3A,B,C U4A,B,C U5A,B,C	104236-G2	23207	IC, Dual Op Amp, Lo Power
U6A,B,C	104247-G1	23207	IC, Dual Op Amp, Low Noise
U7A,B,C U8A,B,C	104241-G1	23207	IC, Dual Op Amp, High Slew Rate
U9A,B,C	104241-G2	23207	IC, Quad Comparator
U10A,B,C U15A,B,C U16A,B,C	104362	23207	IC, Quad Switch
XU5A,B,C XU7A,B,C XU8A,B,C	104927	23207	IC Socket, 8 Pin
XU9A,B,C XU10A,B,C XU15A,B,C XU16A,B,C	104929	23207	IC Socket, 16 Pin

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Digital Board A2, P/N 110666-G2

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
C1,C2,C5,C7-C9,C12-C15,C17,C20,C21,C31-C33,C37-C42,C44,C45	103209-G3	23207	Cap, 0.47 uf, 20%, 50V
C3,C4	104067-G7	23207	Cap, 33 uf, 10%, 16V
C6	104067-G3	23207	Cap, 56 uf, 10%, 6V
C10,C11	104026-G5	23207	Cap, 20 pf, 5%, 500V
C18	104017-G5	23207	Cap, 36 pf, 5%, 500V
C22-C24	104018-G2	23207	Cap, 47 pf, 5%, 500V
C25,C26	104111-G3	23207	Cap, 75 pf, 2%, 500V
C27,C36	104020-G1	23207	Cap, 470 pf, 5%, 500V
C28-C30	104015-G2	23207	Cap, 220 pf, 5%, 500V
C34	104110-G1	23207	Cap, .022 uf, 2%, 50V
C35	104110-G6	23207	Cap, .015 uf, 2%, 50V
C43	104067-G5	23207	Cap, 10 uf, 5%, 6V
CR1-CR3,	104412-G2	23207	Diode, High Speed CR5,CR6 Switching
CR4,CR7	103295	23207	Diode, 6.2V Ref.
Used @ J1A, J1B	2-87348-0	00779	20 Pin Header
R1-R3	RCR07G103J	81349	Res, 10K, 5%, 1/4W
R4,R18	RN55D1005F	81349	Res, 10 Meg, 1%, 1/10W

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Digital Board A2, P/N 110666-G2 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
U29	104200-G3	23207	IC, COS/MOS NAND Gate
U30	104391-G1	23207	IC, Dual CMOS Op-Amp
U31,U32	104362	23207	IC, Quad Switch
U33,U34,U51, U54	104236-G2	23207	IC, Dual Op Amp
U45-U47	104231-G5	23207	IC, Dual One Shot CMOS
U48	104241-G2	23207	IC, Quad Comparator
U52	104250	23207	IC, CMOS Oscillator and 14-Bit Counter
U53	104242-G1	23207	IC, 1 of 8 Analog Mux
XU5,XU15	104933	23207	IC Socket
XU7,XU17	104935	23207	IC Socket
XU18	104934	23207	IC Socket
XU22,XU38, XU42	104928	23207	IC Socket
XU30	104927	23207	IC Socket
XU31,XU32	104929	23207	IC Socket
Y1	107454	23207	Xtal, 5.0688 MHz
Y2	107519	23207	Xtal, 30.72 KHz
Y3	104939	23207	Xtal, Tuning Fork, 12.8 KHz

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Graphics Adapter Board A3, P/N 112985-G1

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
C1A-C,C3A-C	104023-G3	23207	Cap, 36 pf, 2%, 500V
C2A-C,C4A-C	104110-G7	23207	Cap, 0.0047 uf, 2%, 50V
C5A-C,C6A-C	104019-G3	23207	Cap, 300 pf, 5%, 100V
C9A-C,C10A-C, C11A-C,C12A-C, C21,C23,C25-C27	103209-G2	23207	Cap, 0.22 uf, 20%, 50V
C9,C10	104027-G8	23207	Cap, 18 pf, 5%, 500V
C11	103204-G10	23207	Cap, 3.9 uf, 10%, 25V
C12-C15,C18,C19	103209-G3	23207	Cap, 0.47 uf, 20%, 50V
C16	104067-G7	23207	Cap, 33 uf, 10%, 16V
C17	103209-G1	23207	Cap, 0.1 uf, 20%, 50V
C20,C22,C24	104067-G2	23207	Cap, 22 uf, 20%, 35V
CR1A-C,CR2A-C, CR3A-C,CR4A-C	104412-G2	23207	General Purpose Diode
CR5A-C,CR6A-C	101345	23207	Low Leakage Diode
CR7,CR8A-C,CR9A-C	104402-G2	23207	Diode, Zener, 6.2V
CR10,CR11	104404-G4	23207	Diode, Zener, 8.2V
L1A-C,L2A-C	103580-G1	23207	Ferrite Bead
R1A-C,R2A-C	RCR07G103J	81349	Res, 10K, 5%, 1/4W
R3A-C,R4A-C, R5A-C,R6A-C	RCR07G202J	81349	Res, 2K, 5%, 1/4W
R7A-C,R9A-C	RN55C4871F	81349	Res, 4.87K, 1%, 1/10W
R8A-C,R32	104719-G6	23207	Res, Var, 1K, 10%, 1/2W

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Graphics Adapter Board A3, P/N 112985-G1 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
R10A-C,R12A-C	RN55C5111F	81349	Res, 5.11K, 1%, 1/10W
R11A-C	104719-G1	23207	Res, Var, 500-Ohm, 10%, 1/2W
R13A-C	RN55C4991F	81349	Res, 4.99K, 1%, 1/10W
R14A-C,R15A-C, R21A-C,R26A-C	RN55C2002F	81349	Res, 20K, 1%, 1/10W
R16A-C,R31	RN55C1002F	81349	Res, 10K, 1%, 1/10W
R17A-C	RCR07G431J	81349	Res, 430-Ohm, 5%, 1/4W
R18A-C,R23A-C	RN55C6191F	81349	Res, 6.19K, 1%, 1/10W
R19A-C,R24A-C	RN55C1502F	81349	Res, 15K, 1%, 1/10W
R20A-C,R25A-C	104719-G8	23207	Res, Var, 2K, 10%, 1/2W
R22A-C,R27A-C	RN55C6651F	81349	Res, 6.65K, 1%, 1/10W
R28	RCR07G203J	81349	Res, 20K, 5%, 1/4W
R29	RN55C6191F	81349	Res, 6.19K, 1%, 1/10W
R30	RN55C4421F	81349	Res, 4.42K, 1%, 1/10W
R33	RN55C8061F	81349	Res, 8.06K, 1%, 1/10W
R34	RCR07G104J	81349	Res, 100K, 5%, 1/4W
R35,R36	RCR07G432J	81349	Res, 4.3K, 5%, 1/4W
RN1A-C,RN2A-C	104711	23207	Resistor Network
U1A-C,U2A-C	104247-G1	23207	I.C., Dual Op Amp
U3A-C	104362	23207	I.C., Quad Switch
U4A-C,U5A-C,U21	104236-G2	23207	I.C., Dual Op Amp

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Graphics Adapter Board A3, P/N 112985-G1 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
U6	104269-G4	23207	I.C., Microprocessor
U7	104271-G2	23207	I.C., Octal Latch
U8,U9	112026-G1	23207	I.C., A/D Converter
U10	112027-G1	23207	I.C., Dual 4-Bit MUX
U11	104231-G5	23207	I.C., Dual One-Shot
U12,U13,U15, U23,U24,U38	104290-G2	23207	I.C., 1 of 8 Decoder
U14	104392-G1	23207	I.C., Quad 2-Input NAND
U16,U17,U36	104295-G1	23207	I.C., Static RAM
U18	See PROM Program Listing 105909		I.C., EPROM 8K x 8
U19,U20	104392-G3	23207	I.C., Quad 2-Input OR
U22	104290-G3	23207	I.C., XCVR, 8-Bit
U25	104392-G7	23207	I.C., Octal Buffer
U26-U30	104290-G4	23207	I.C., Octal "D" Flip-Flop
U31-U33	104392-G2	23207	I.C., Dual "D" Flip-Flop
U34	104271-G9	23207	I.C., Hex Inverter
U35	See PROM Program Listing 105909		I.C., EPROM, 8K x 8
U37	104392-G9	23207	I.C., Quad AND
Y1	110729-G8	23207	Crystal, 8.000 MHz
Used at U8,U9	110749-G5	23207	I.C., Socket, Sealed, 20-Pin

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

REPLACEABLE PARTS LIST

626-PA-6030

Graphics Adapter Board A3, P/N 112985-G1 (Cont'd)

REFERENCE DESIGNATION	PART NO.	MAN. CODE NO.	DESCRIPTION
Used at U16,U17,U18, U35,U36	110749-G8	23207	I.C., Socket, Sealed, 28-Pin
Used at U6	110749-G9	23207	I.C., Socket, Sealed 40-Pin

Proprietary Information -- Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

SECTION VII

SCHEMATIC DIAGRAMS AND ASSEMBLY DRAWINGS

This section contains the schematic diagrams and assembly drawings for the 6030 plug-in. The schematic diagrams (figs. 7-5 through 7-7) supplement the Theory of Operation section; the assembly drawings (figs. 7-1 through 7-3) illustrate and locate the parts referenced in the Replaceable Parts List of this manual.

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

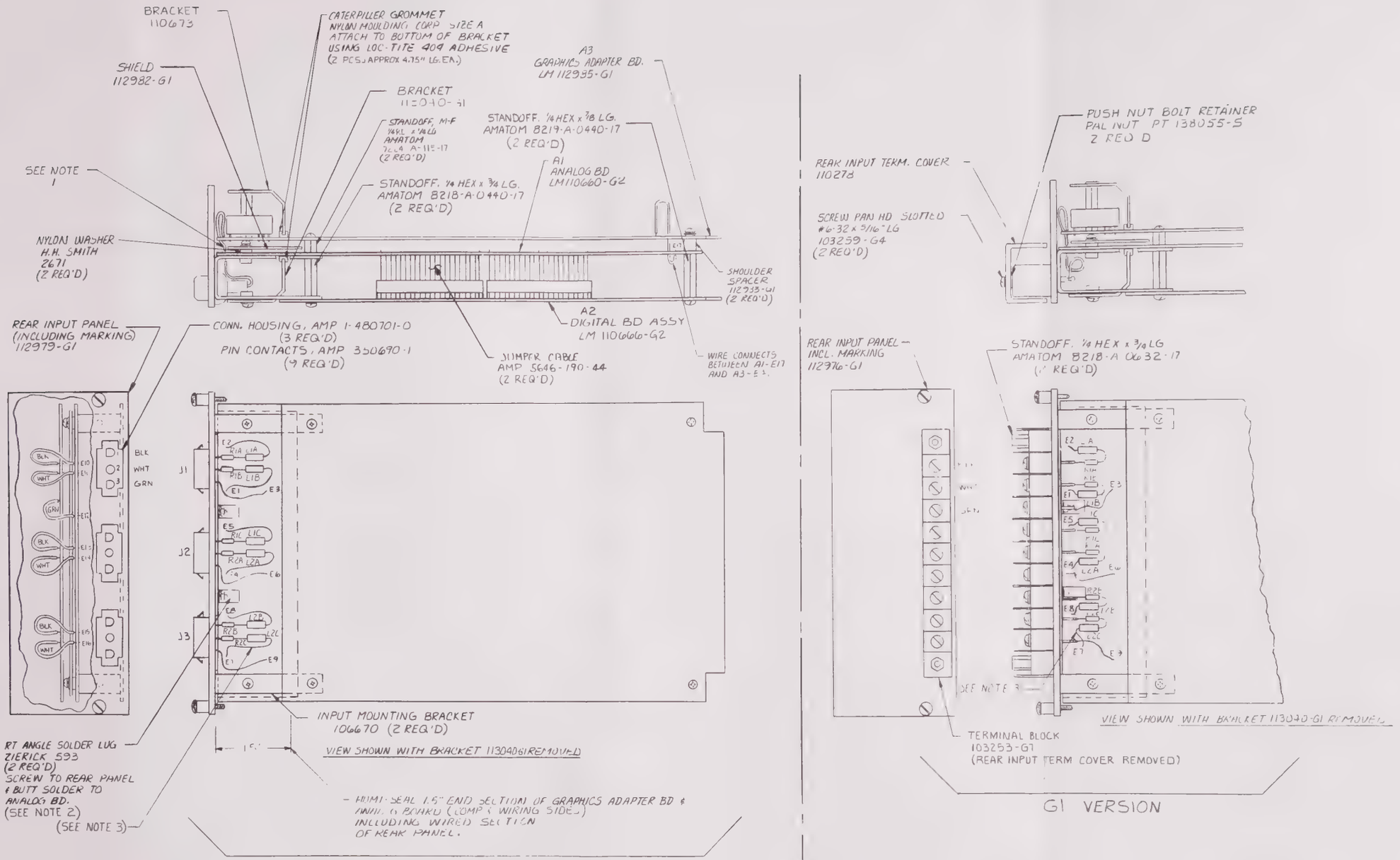
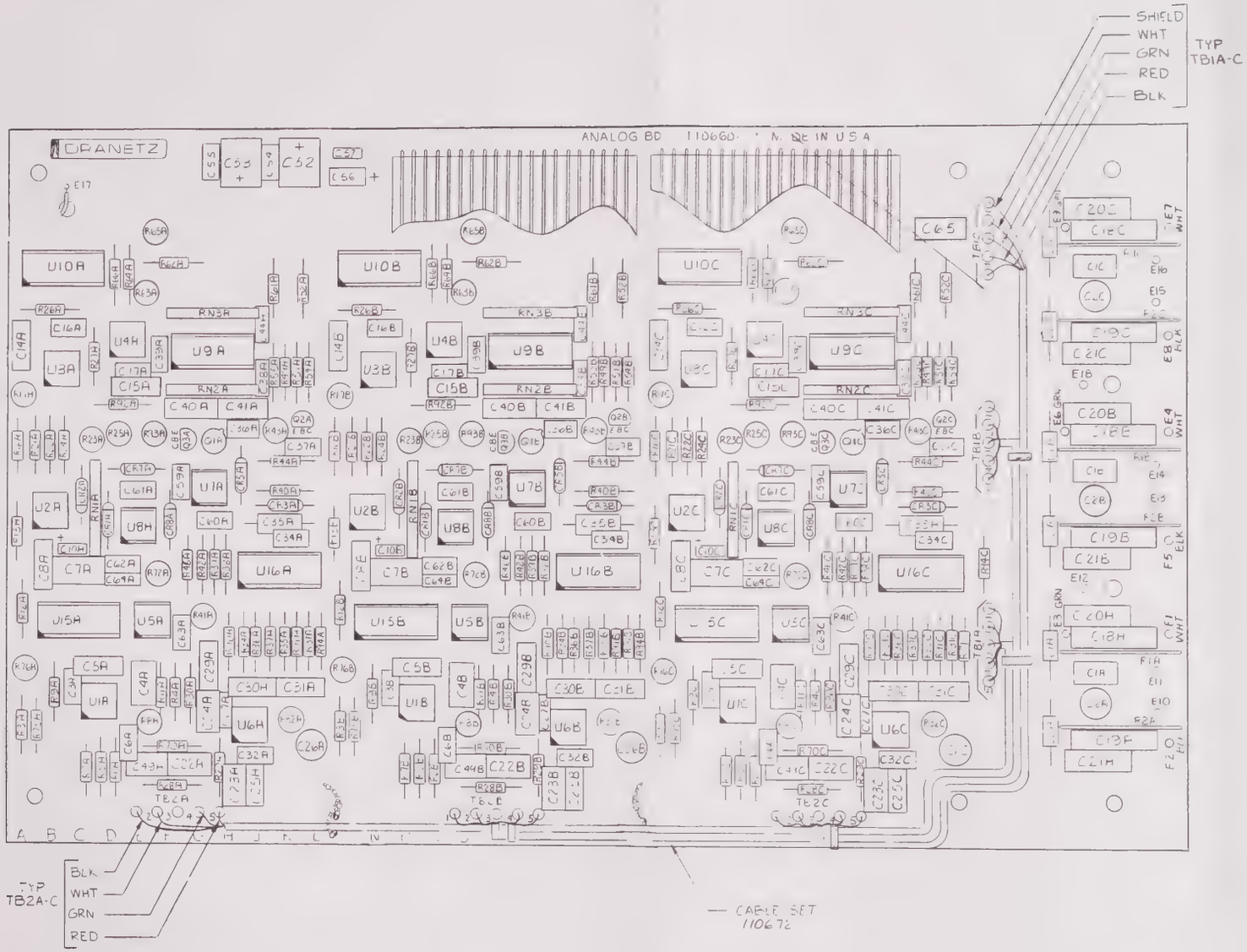

BRACKET 110673
CATERPILLER GROMMET NYLON MOULDING CORP SIZE A ATTACH TO BOTTOM OF BRACKET USING LOC-TITE 409 ADHESIVE (2 PCS, APPROX 4.75" LG. EA.)
A3 GRAPHICS ADAPTER BD. LM 112935-G1
SHIELD 112982-G1
BRACKET 110040-G1
STANDOFF, M-F 1/4 HEX x 1/4 LG AMATOM 7264 A-115-17 (2 REQ'D)
STANDOFF. 1/4 HEX x 3/8 LG. AMATOM 8219-A-0440-17 (2 REQ'D)
A1 ANALOG BD LM110660-G2
SEE NOTE 1
STANDOFF. 1/4 HEX x 3/4 LG. AMATOM 8218-A-0440-17 (2 REQ'D)
NYLON WASHER H.H. SMITH 2671 (2 REQ'D)
SHOULDER SPACER 112933-G1 (2 REQ'D)
A2 DIGITAL BD ASSY LM 110666-G2
REAR INPUT PANEL (INCLUDING MARKING) 112979-G1
CONN. HOUSING, AMP 1-480701-0 (3 REQ'D)
PIN CONTACTS, AMP 350690-1 (9 REQ'D)
JUMPER CABLE AMP 5646-190-44 (2 REQ'D)
WIRE CONNECTS BETWEEN A1-E17 AND A3-E1.
BLK
WHT
GRN
J1
J2
J3
INPUT MOUNTING BRACKET 106670 (2 REQ'D)
VIEW SHOWN WITH BRACKET 113040G1 REMOVED
RT ANGLE SOLDER LUG ZIERICK 593 (2 REQ'D) SCREW TO REAR PANEL & BUTT SOLDER TO ANALOG BD. (SEE NOTE 2)
(SEE NOTE 3)
- MIMI-SEAL 1.5" END SECTION OF GRAPHICS ADAPTER BD & ANAL. G BOARD (COMP & WIRING SIDES) INCLUDING WIRED SECTION OF REAR PANEL.
G2 VERSION
PUSH NUT BOLT RETAINER PAL NUT PT 138055-5 2 REQ'D
REAR INPUT TERM. COVER 110278
SCREW PAN HD SLOTTED #6-32 x 5/16" LG 103259-G4 (2 REQ'D)
REAR INPUT PANEL INCL. MARKING 112976-G1
STANDOFF. 1/4 HEX x 3/8 LG AMATOM 8218-A 0632-17 (4 REQ'D)
SEE NOTE 3
TERMINAL BLOCK 103253-G1 (REAR INPUT TERM COVER REMOVED)
VIEW SHOWN WITH BRACKET 113040-G1 REMOVED
G1 VERSION

Figure 7-1. 626-PA-6030 3-Phase Graphic AC Monitor, Main Assembly Drawing 112975-G( ), Rev. B

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

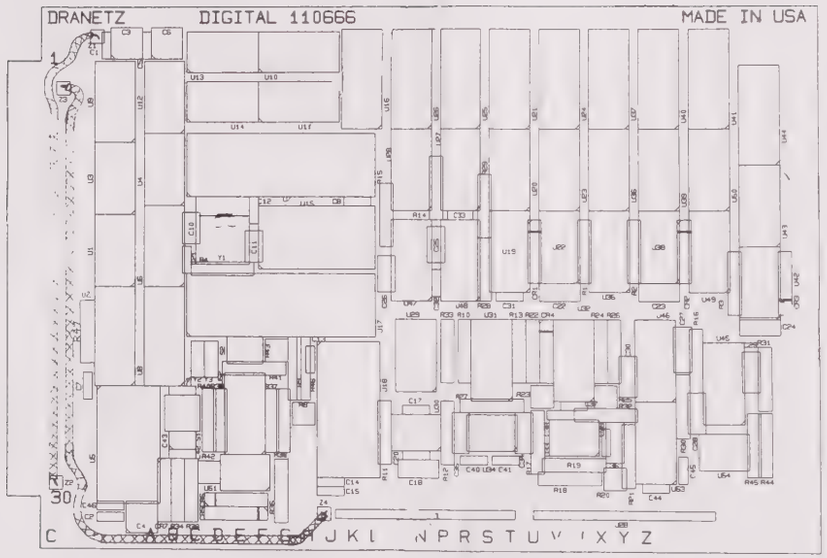


"G" LEVEL CHART

REF DESIG	G1	G2
C14,A,B,C	.0	.022
R9,A,B,C	182K, ±1%, 1/10W	1.1M, ±1%, 1/10W
R11,A,B,C	51.1K, ±1%, 1/10W	332K, ±1%, 1/10W
R12,A,B,C	133K, ±1%, 1/10W	909K, ±1%, 1/10W
R13,A,B,C	48.7K, ±1%, 1/10W	324K, ±1%, 1/10W
R26,A,B,C	340K, ±1%, 1/10W	402K, ±1%, 1/10W
R34,A,B,C R35,A,B,C	383K, ±1%, 1/10W	301K, ±1%, 1/10W
R36,A,B,C	102K, ±1%, 1/10W	274K, ±1%, 1/10W
R37,A,B,C	9.53K, ±1%, 1/10W	1.5K, ±1%, 1/10W
R40,A,B,C R41,A,B,C	392K, ±1%, 1/10W	1.47M, ±1%, 1/10W
R92,A,B,C	40.2K, ±1%, 1/10W	86.4K, ±1%, 1/10W
R93,A,B,C	50K, ±10%, 1/2W	100K, ±10%, 1/2W

Figure 7-2. 6030 Analog Board, Assembly Drawing 110660-G2 (Rev. J)

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.



"G" LEVEL CHART

REF DESIG	G1	G2
C34	.01	.022
R22	750K ±1% .1/10W	665K ±1% .1/10W
R24	634K ±1% .1/10W	536K ±1% .1/10W

Figure 7-3. 6030 Digital Board, Assembly Drawing 110666-G2, Rev. H

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

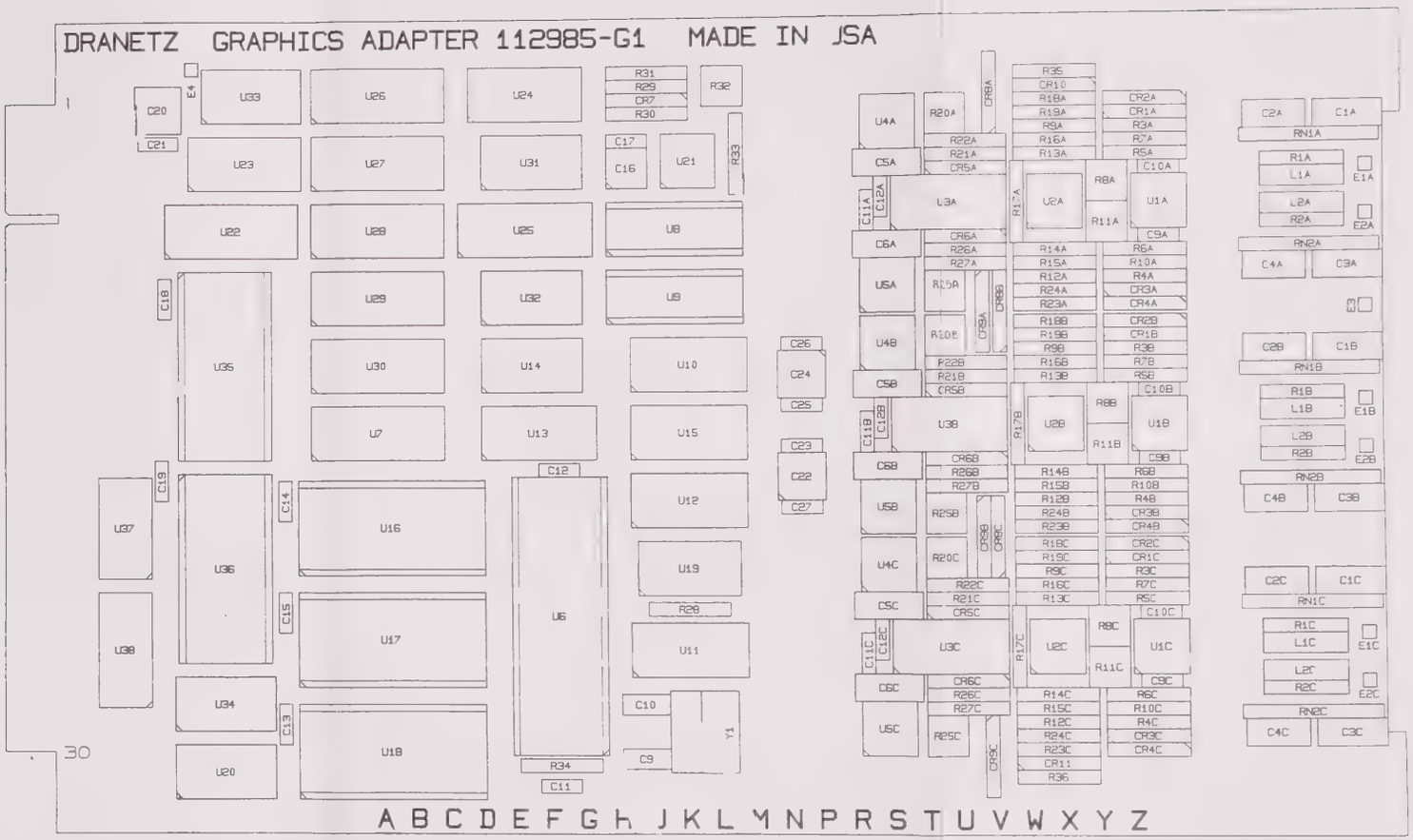
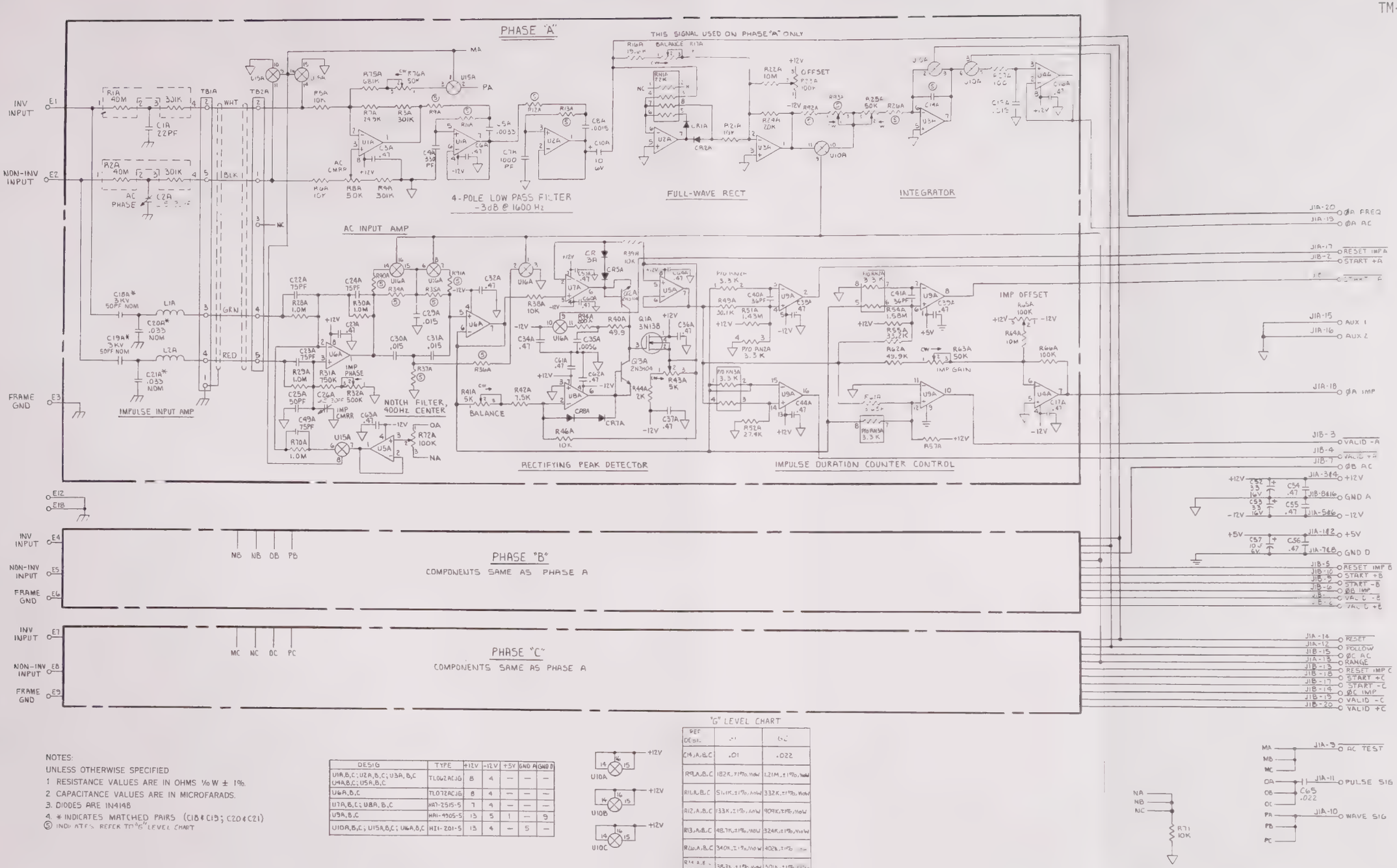


Figure 7-4. 6030 Graphics Adapter Board, Assembly Drawing 112985-G1, Rev. A

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.



NOTES:
UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS ⅛W ± 1%
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. DIODES ARE IN4148
4. * INDICATES MATCHED PAIRS (C18&C19; C20&C21)
⑤ INDICATES REFER TO "G" LEVEL CHART

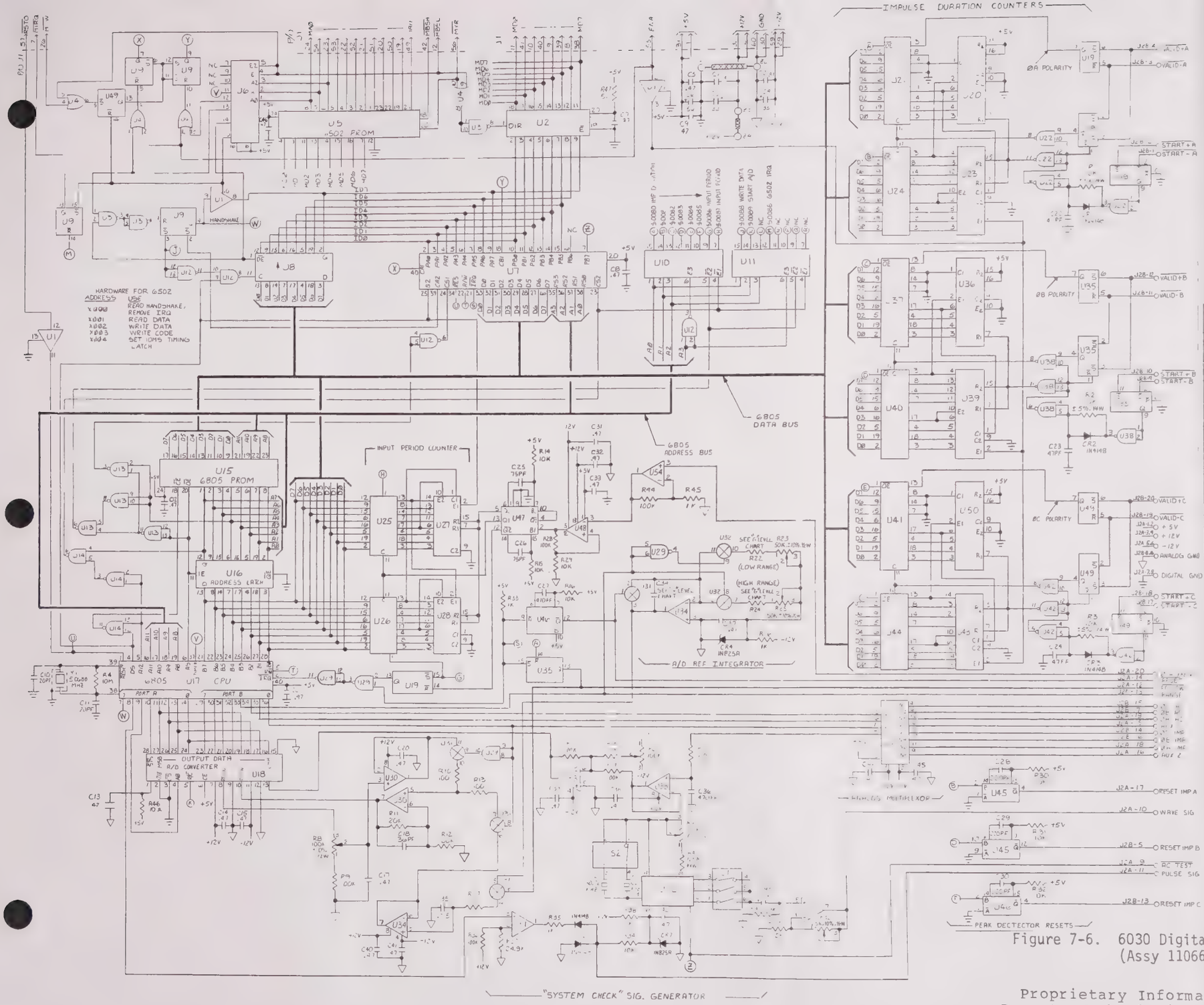
DESIG	TYPE	+12V	-12V	+5V	GND A	GND B
U1A,B,C; U2A,B,C; U3A,B,C U4A,B,C; U5A,B,C	TL062ACJG	8	4	—	—	—
U6A,B,C	TL072ACJG	8	4	—	—	—
U7A,B,C; U8A,B,C	HA7-2515-5	7	4	—	—	—
U9A,B,C	HA1-4905-5	13	5	1	—	9
U10A,B,C; U15A,B,C; U16A,B,C	HI1-201-5	13	4	—	5	—

"G" LEVEL CHART

REF DESIG.	-1	-2
C14,A,B,C	.01	.022
R9A,B,C	182K, ±1%, ¼W	1.21M, ±1%, ¼W
R11,A,B,C	511K, ±1%, ¼W	332K, ±1%, ¼W
R12,A,B,C	133K, ±1%, ¼W	909K, ±1%, ¼W
R13,A,B,C	48.7K, ±1%, ¼W	324K, ±1%, ¼W
R16,A,B,C	340K, ±1%, ¼W	402K, ±1%
R14,A,B, R15,A,B,C	383K, ±1%, ¼W	301K, ±1%, ¼W
R34,A,B,C	102K, ±1%, ¼W	374K, ±1%, ¼W
R37,A,B,C	49.5K, ±1%, ¼W	75K, ±1%, ¼W
R90,A,B,C R91,A,B,C	392K, ±1%, ¼W	1.47M, ±1%, ¼W
R92,A,B,C	40.2K, ±1%, ¼W	49.9K, ±1%, ¼W
R93,A,B,C	50K, ±10%, ½W	100K, ±10%, ½W

Figure 7-5. 6030 Analog Board A1, Schematic Diagram (Assy 110660-G2; Schem. 110665-G2, Rev. J)

Proprietary Information; Copyright © 1987 Dranetz Technologies, Inc. All Rights Reserved.



'G' LEVEL CHART

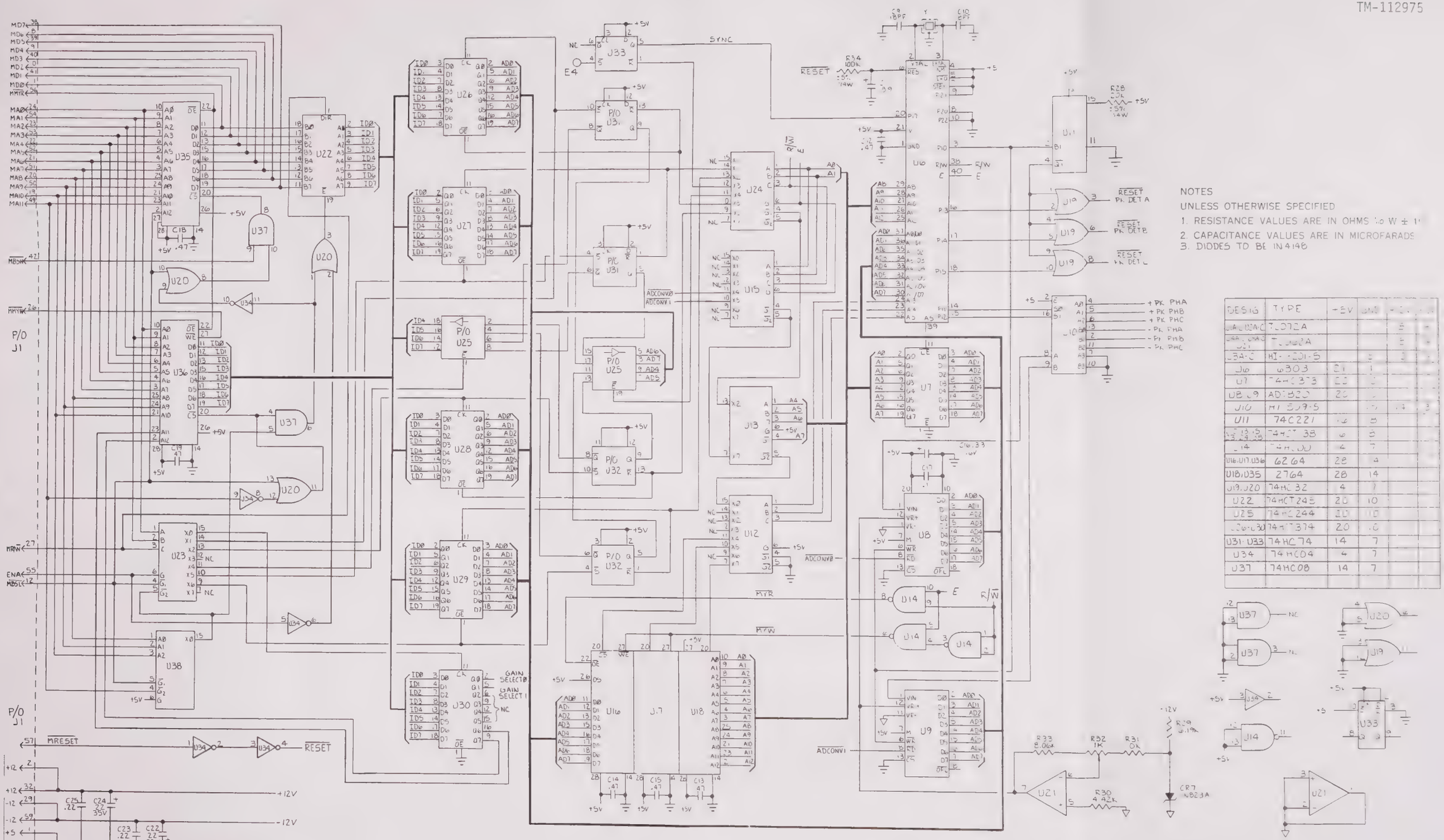
REF DESIG	
U22	
U24	
R22	750K, ±1%, ¼W
R24	634K, ±1%, ¼W
R23	665K, ±1%, ¼W
	536K, ±1%, ¼W

REF DESIG	TYPE	+12V	-12V	+5V	GND	NC
U1	SN74LS125			14	7	
U2	74LS245			20	10	
U3, U12, U13, U14	SN74LS00			14	7	
U4	SN74LS32			14	7	
U5, U15	D2732			24	12	
U6, U10, U11	SN74LS138			16	8	
U7	SY6522A			20	1	
U8, U21, U24, U25, U26, U37, U40, U41, U44	MM74C374			20	10	
U9, U19, U35, U49	SN74LS279			16	8	
U16	MM74C373			20	10	
U17	MC146805E2			40	20	
U18	ADS142KD	7	11			15, 9
U20, U23, U27, U28, U36, U39, U43, U50	MC14520			16	8	
U22, U38, U42	74SC00			14	7	
U29	CD4011			14	7	
U30	ICL7621	8				4
U31, U32	HI1-201-5	13	4			
U33, U34, U51, U54	TL062CH	8	4			
U45, U46, U47	MM74C221			16	8	
U48	HA1-4905-5	13	5	1	9	
U52	CD4066BF					8
U53	HI1-0508-5	13	5			14

NOTES
UNLESS OTHERWISE SPECIFIED
1. RESISTANCE VALUES ARE IN OHMS ¼ W ± 5%
2. CAPACITANCE VALUES ARE IN MICROFARADS
3. ALL LETTERS IN H CIRCLE INDICATE AN INTERCONNECTION
4. SWITCHES ARE SHOWN IN 400HZ POSITION

Figure 7-6. 6030 Digital Board A2, Schematic Diagram (Assy 110666-G2; Schem 110671-G2, Rev. H)

Proprietary Information; Copyright © 1987 Dranetz Technologies, Inc. All Rights Reserved.



DESIG	TYPE	-5V	GND	+5	+12
U1A,U2A,U3A	74LS32A			14	
U4A,U5A,U6A	74LS08A			14	
U8A-C	HI-5051-5		5	3	
J10	6303	21	1		
U7	74HCT373	20	10		
U8,U9	AD7820	28	14		
J10	MI 5049-5		12	14	3
U11	74C221	16	8		
U12,U13,U28,U29	74HCT 38	16	8		
U14	74HC00	4	7		
U16,U17,U36	6264	28	14		
U18,U35	2764	28	14		
U19,U20	74HC32	14	7		
U22	74HCT245	20	10		
U25	74HC244	20	10		
U26-U30	74HCT374	20	10		
U31-U33	74HC74	14	7		
U34	74HC04	14	7		
U37	74HC08	14	7		

Figure 7-7. Graphics Adapter Board, Schematic Diagram (Sheet 1 of 2)
(Assy 112985-G1; Schem 112990-G1, Rev. A)

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

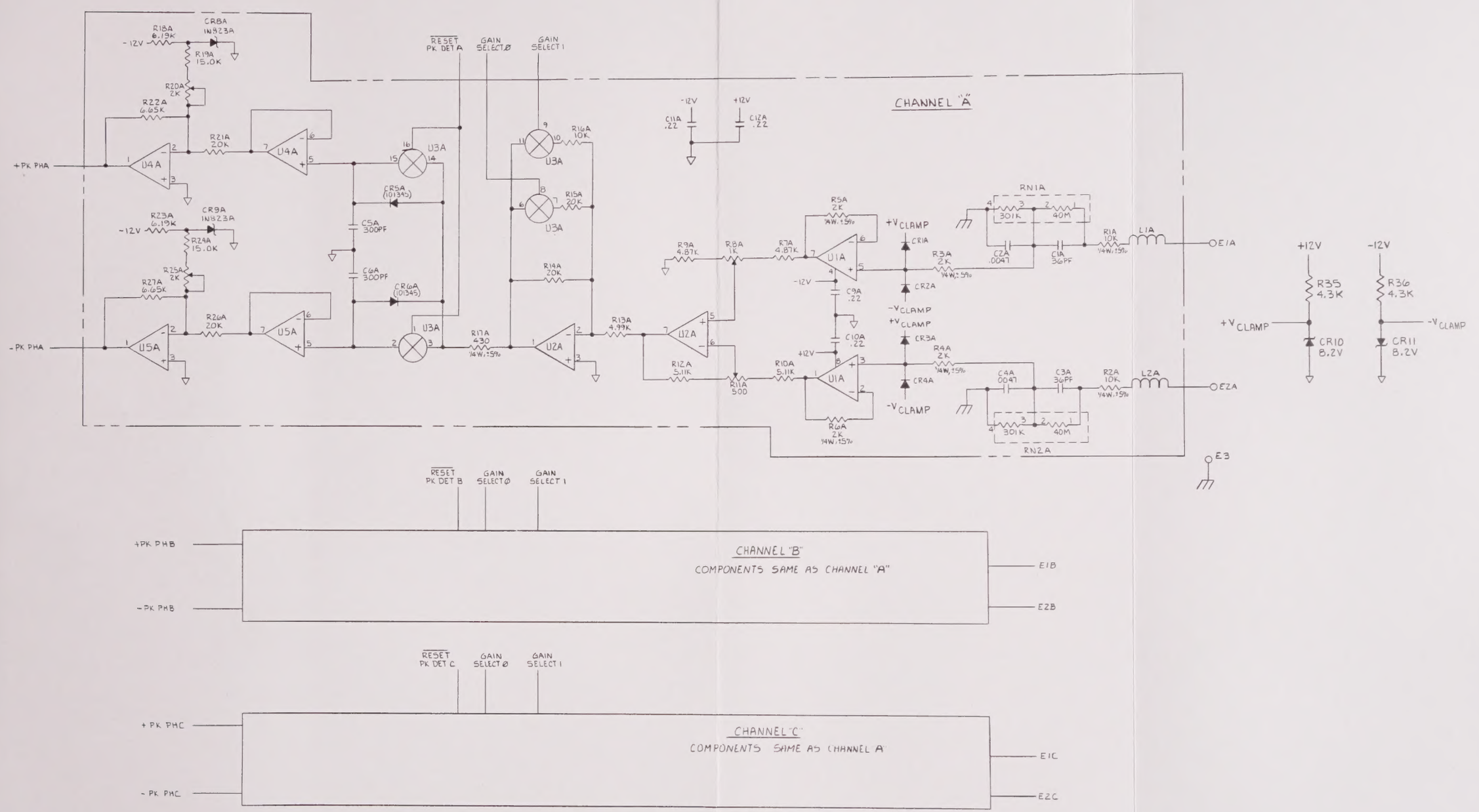


Figure 7-7. Graphics Adapter Board, Schematic Diagram (Sheet 2 of 2)
(Assy 112985-G1; Schem 112990-G1, Rev. A)

Proprietary Information; Copyright © 1987
Dranetz Technologies, Inc. All Rights Reserved.

www.manualsplus.com
1002137

DUO-TANG®
53530